



SPECTRUM

SYSTEMENTWICKLUNG MICROELECTRONIC GMBH

MX.70xx - 32 bit fast digital I/O with TTL levels

- **PXI 3U / CompactPCI 3U format**
- **1, 2, 4, 8, 16 bit or 32 bit digital I/O**
- **1 kS/s up to 125 MS/s at 16 bit**
- **1 kS/s up to 60 MS/s at 32 bit**
- **110 Ohm input impedance selectable**
- **3.3 V and 5 V TTL compatible I/O**
- **Up to 128 MByte memory**
- **FIFO mode for input and output**
- **Pattern/Edge/Pulsewidth trigger**
- **Synchronization possible**
- **Windows program SBench 5.x included**



Product range overview

Model	1-4 bit	8 bit	16 bit	32 bit
MX.7005	125 MS/s	125 MS/s	125 MS/s	
MX.7010		125 MS/s	125 MS/s	
MX.7011		125 MS/s	125 MS/s	60 MS/s

Software/Drivers

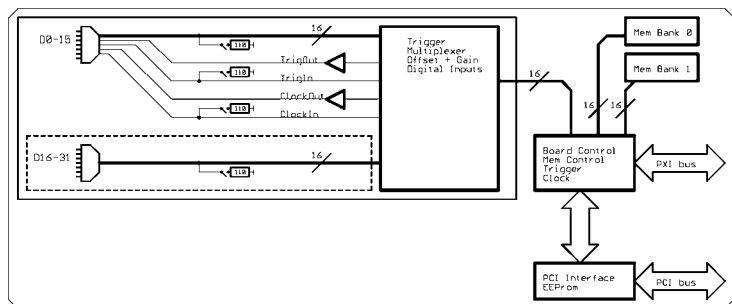
A large number of drivers and examples are delivered with the board or are available as an option:

- Windows 98/ME/NT/2000/XP - drivers
- Linux - drivers
- SBench 5.2
- Streaming Software SPviewIT 6.1 (as option, recording only)
- Microsoft Visual C++ examples
- Borland Delphi examples
- Microsoft Visual Basic examples
- Microsoft Excel examples
- LabWindows/CVI examples
- FlexPro support with SBench
- LabVIEW - drivers (as option)
- DASYLab - drivers (as option)
- MATLAB - drivers (as option)
- Agilent VEE - drivers (as option)

General Information

The MX.70xx series of fast digital I/O boards offer a resolution between 1 bit and 32 bit with a maximum samplerate of 125 MS/s (60 MS/s). Every 16 bit / 32 bit of the board could be separately programmed for input or output. The on-board memory of up to 128 MByte could be completely used for recording or re-playing digital data. Alternatively the MX.70xx could be used in FIFO mode. Then data is transferred on-line to PC memory or hard disk. The internal standard synchronisation bus allows synchronisation of several MX.xxxx boards. Therefore the MX.70xx board could be used as an enlargement to analogue boards.

Hardware block diagram



Software programmable parameters

Samplerate	1 kS/s to max samplerate, external clock, ref clock, PXI clock
Direction	Input/Output for each module
Input impedance	110 Ohm / 50 kOhm for each channel
Clock mode	internal PLL, internal quartz, external, external divided, external reference clock, PXI reference clock
Clock impedance	110 Ohm / 50 kOhm
Trigger impedance	110 Ohm / 50 kOhm
Trigger pulsewidth	1 to 256 samples in steps of 1
Trigger mode	Pattern and mask, edge, external TTL, software, PXI Line[5..0], PXI Startrigger
Pattern and mask	32 bit / 64 bit wide: 0 pattern, 1 pattern, don't care or edge
Memory depth	32 up to installed memory in steps of 32
Posttrigger	32 up to 128 M in steps of 32
Multiple Recording segmentsize	32 up to installed memory / 2 in steps of 32

Application examples

Semiconductor test	Production test	Pattern generator
A/D data acquisition	Logic analyser	Pattern recognition

Possibilities and options

PXI bus

The PXI bus (PCI eXtension for instrumentation) offers a variety of additional normed possibilities for synchronising different components in one system. It is possible to connect several Spectrum cards with each other as well as to connect a Spectrum card with cards of other manufacturers.

PXI reference clock

The card is able to use the 10 MHz reference clock that is supplied by the PXI system. Enabled by software the PXI reference clock is feeded in the on-board PLL. This feature allows the cards to run with a fixed phase relation.

PXI trigger

The Spectrum cards support star trigger as well as the PXI trigger bus. using a simple software command one or more trigger lines can be used as trigger source. This feature allows the easy setup of OR connected triggers from different cards.

FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

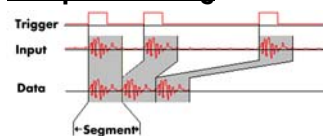
Pattern trigger

For every bit of the digital input the pattern trigger defines individually the expected level or sets the bit to „don't care“. In combination with pulsewidth counter and edge detection the pattern trigger could be used to recognise a huge variety of trigger events.

External trigger I/O

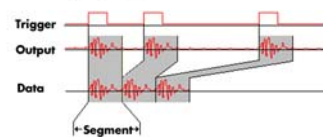
All boards could be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulsewidth. An internally recognised trigger event could - activated by software - routed to the output connector to start external instruments.

Multiple Recording



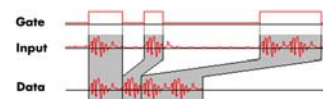
The Multiple Recording option allows the recording of several trigger events without restarting the hardware. With this option very fast repetition rates could be achieved. The on-board memory is divided in several segments of same size. Each of them is filled with data if a trigger event occurs.

Multiple Replay



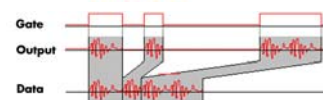
The Multiple Replay option allows the fast repetition output on several trigger events without restarting the hardware. With this option very fast repetition rates could be achieved. The on-board memory is divided in several segments of same size. Each of them is generated if a trigger event occurs.

Gated Sampling



The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level.

Gated Replay

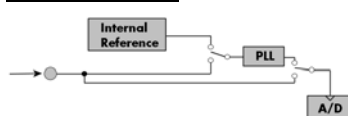


The Gated Sampling option allows data replay controlled by an external gate signal. Data is only replayed if the gate signal has a programmed level.

External clock I/O

Using an external connector a sampling clock could be fed in from an external system. It's also possible to put out the internally used sampling clock to synchronise external equipment to this clock.

Reference clock



The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Singleshot output

When singleshot output is activated the data of the on-board memory is replayed exactly one time. As trigger source one can use the external TTL trigger or the software trigger.

Continuous output

When continuous output is activated the data of the on-board memory is replayed continuously until a stop command is executed. As trigger source one can use the external TTL trigger or the software trigger.

1-4 bits mode

On the model 7005 it is also possible to use just 1, 2 or 4 bits for acquisition or replay. In 1 bit mode the 8 times higher memory is then available, at 2 bits mode it is 4 times higher and at 4 bits mode it is double. This enlarges the recording/replay time in on-board memory and it reduces the transfer rate when using FIFO mode.

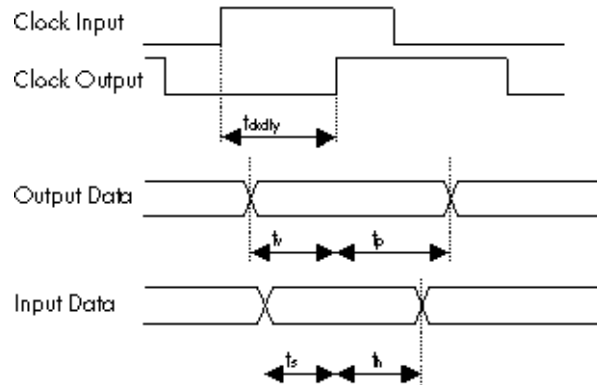
Technical Data

Internal samplerate	1 kS/s up to 125 MS/s	Dimension	160 mm x 233 mm (Standard 3U)
External samplerate	DC up to 125 MS/s	Width (MX.7005, MX.7010)	1 slot
Input impedance	110 Ohm / 50 kOhm 15 pF	Width (MX.7011)	2 slots
110 Ohm termination voltage	2.5V	Connector	40 pol half pitch (Hirose FX2 series)
Signal level (data, trigger, clock)	3.3 V/ 5 V TTL compatible	Operating temperature	0°C - 50°C
Data input current sink (no termination)	0.0 V 3.3 V 5.0 V -1.0 µA +1.0 µA +20.0 µA	Storage temperature	-10°C - 70°C
Clock / trigger input current sink (no termination)	± 1.0 µA	Humidity	10% to 90%
Multi: Trigger to 1st sample delay	fixed		
Multi: Recovery time	< 20 samples (16 - 64 bit)		
ext. Trigger accuracy (samples)	32 bit 16 bit 8 bit 4 bit 2 bit 1 bit 1 1 2 4 8 16		
int. Trigger accuracy (samples)	1 1 2 4 8 16		
Trigger input: Standard TTL level	Low: -0.5 > level < 0.8 V High: 2.0 V > level < 5.5 V Trigger pulse must be valid ≥ 2 clock periods.	Clock input: Standard TTL level	Low: -0.5 > level < 0.8 V High: 2.0 V > level < 5.5 V Rising edge is used. Required duty cycle: 50% ± 5%
Trigger output	Standard TTL, capable of driving 50 Ohm. Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -32 mA) One positive edge after the first internal trigger	Clock output	Standard TTL, capable of driving 50 Ohm Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -32 mA)

Power consumption (maximum value)	Full speed				Power down mode			
	+3,3 V	+5 V	+12 V	-12 V	+3,3 V	+5 V	+12 V	-12 V
MX.7005 (16 bit output @ 125 MS/s in 110 Ohm)	0 A	3.5 A (17.5 W)	0 A	0 A	0 A	1.5 A (7.5 W)	0 A	0 A
MX.7010 (16 bit output @ 125 MS/s in 110 Ohm)	0 A	3.5 A (17.5 W)	0 A	0 A	0 A	1.5 A (7.5 W)	0 A	0 A
MX.7011 (32 bit output @ 60 MS/s in 110 Ohm)	0 A	3.0 A (15.0 W)	0 A	0 A	0 A	1.5 A (7.5 W)	0 A	0 A

For detailed information on the different modes for external clocking please refer to the dedicated chapter in the hardware manual for the boards of the 70xx series.

Delay time	External Clocking Mode		
	SINGLE	BURST S	BURST M
t_{ckdly}	20 ns	30 ns	< 1 ns
t_v	> 350 ns	> 150 ns	> 2.5 ns
t_p	> 2.5 ns	> 2.5 ns	> 2.5 ns
t_s	≤ 3.0 ns	≤ 3.0 ns	≤ 3.0 ns
t_{vh}	≤ 1.0 ns	≤ 1.0 ns	≤ 1.0 ns



Order information

Order No	Description	Order No	Description
MX7005	MX.7005 with 16 MByte (128 MBit) memory, cables and drivers	MX7xxx-32M	Option: 32 MByte memory instead of 16 MByte standard mem
MX7010	MX.7010 with 16 MByte (128 MBit) memory, cables and drivers	MX7xxx-64M	Option: 64 MByte memory instead of 16 MByte standard mem
MX7011	MX.7011 with 16 MByte (128 MBit) memory, cables and drivers	MX7xxx-128M	Option: 128 MByte memory instead of 16 MByte standard mem
MX7xxx-mr	Option Multiple Replay: Memory segmentation	MX7xxx-up	Additional handling costs for later memory upgrade
MX7xxx-gs	Option Gated Sampling: Gate signal controls replay	MX70xx-dl	DASYLab driver for MX.70xx series
MXxxxx-dcab	Additional 40 pole flat ribbon cable with IDC socket connector, ca. 1 m	MX70xx-hp	VEE driver for MX.70xx series
MXxxxx-dcab2	Additional 40 pole flat ribbon cable withFx2 connector, ca. 1 m	MX70xx-lv	LabVIEW driver for MX.70xx series
		MATLAB	MATLAB driver for all MI.xxxx, MC.xxxx and MX.xxxx series.

technical changes and printing errors possible