SPECTRUM
SYSTEMENTWICKLUNG MICROELECTRONIC GMBH

MX.45xx - two channel 16 bit high-speed A/D

- **PXI 3U / CompactPCI 3U format**
- **Fastest 16 bit A/D converter board**
- **Models with 200 kS/s, 500 kS/s or 1 MS/s**
- **Simultaneously sampling on both channels**
- **4 input ranges: ±1 V up to ± 10 V**
- **Differential / single-ended selectable**
- **Up to 64 MSample memory**
- **FIFO mode**
- **Window and pulsewidth trigger**
- **Input offset up to ±100%**
- **Synchronization possible**
- **Windows program SBench 5.x included**

Product range overview

Model	1 channel	2 channels
MX.4520	200 kS/s	200 kS/s
MX.4530	500 kS/S	500 kS/s
MX.4540	1 MS/s	1 MS/s

Software/Drivers

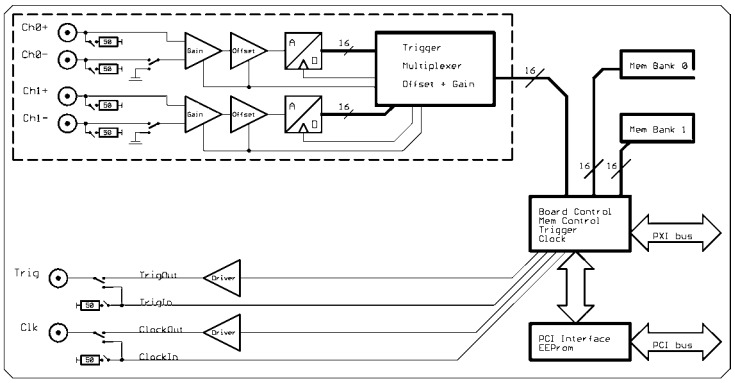
A large number of drivers and examples are delivered with the board or are available as an option:

- Windows 98/ME/NT/2000/XP - drivers
- Linux - drivers
- SBench 5.2
- Streaming Software SPviewIT 6.2(as option)
- Microsoft Visual C++ examples
- Borland Delphi examples
- Microsoft Visual Basic examples
- Microsoft Excel examples
- LabWindows/CVI examples
- FlexPro support with SBench
- LabVIEW - drivers (as option)
- DASYLab - drivers (as option)
- MATLAB - drivers (as option)
- Agilent VEE - drivers (as option)

General Information

The MX.45xx for the first time offers full 16 bit resolution synchronously on two channels at very high samplerates. Every channel has its own amplifier and A/D converter. This eliminates the problems known from multiplexed systems like phase error between the channels or high crosstalk. Every input channel could be offset calibrated using the software. The user will find easily a matching solution from the three offered models. These versions are working with samplerates of 200 kS/s, 500 kS/s or 1 MS/s. The boards can also be updated to a multi-channel system using the internal synchronization bus.

Hardware block diagram



Software programmable parameters

Samplerate	1 kS/s to max samplerate, external clock, ref clock, PXI clock
Input Range	±1 V, ±2 V, ±5 V, ±10 V
Input impedance	50 Ohm / 1 MOhm
Input type	Single-ended, differential
Input Offset	±100% in steps of 1%
Clock mode	internal PLL, internal quartz, external, external divided, external reference clock, PXI reference clock
Clock impedance	50 Ohm / 1 MOhm
Trigger impedance	50 Ohm / 1 MOhm
Trigger mode	Channel, External, Software, Auto, Windows, Pulse, PXI Line[5..0], PXI Startrigger
Trigger level	1/2048 to 2047/2048 of input range
Trigger edge	rising edge, falling edge or both edges
Trigger pulsewidth	1 to 255 samples in steps of 1 sample
Memory depth	32 up to installed memory in steps of 32
Posttrigger	32 up to 128 M in steps of 32
Multiple Recording segmentsize	32 up to installed memory / 2 in steps of 32

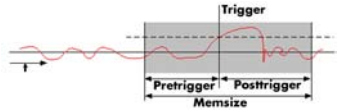
SPECTRUM SYSTEMENTWICKLUNG MICROELECTRONIC GMBH · AHRENSFELDER WEG 13-17 · 22927 GROSSHANSDORF · GERMANY
PHONE: +49 (0)4102-6956-0 · FAX: +49 (0)4102-6956-66 · E-MAIL: info@spec.de · INTERNET: http://www.spec.de

Possibilities and options

PXI bus
The PXI bus (PCI eXtension for instrumentation) offers a variety of additional normed possibilities for synchronising different components in one system. It is posible to connect several Spectrum cards with each other as well as to connect a Spectrum card with cards of other manufacturers.

PXI reference clock
The card is able to use the 10 MHz reference clock that is supplied by the PXI system. Enabled by software the PXI reference clock is feeded in the on-board PLL. This feature allows the cards to run with a fixed phase relation.

PXI trigger
The Spectrum cards support star trigger as well as the PXI trigger bus. using a simple software commend one or more trigger lines can be used as trigger source. This feature allows the easy setup of OR connected triggers from different cards.

Ring buffer mode


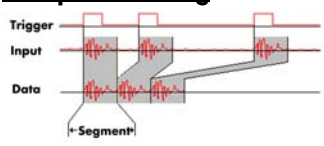
The ring buffer mode is the standard mode of all oscilloscope boards. Data is written in a ring memory of the board until a trigger event is detected. After the event the posttrigger values are recorded. Because of this continuously recording in a ring buffer there are also samples prior to the trigger event visible: Pretrigger = Memsize - Posttrigger.

FIFO mode
The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

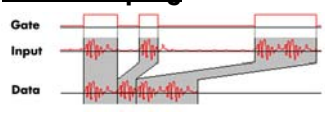
Channel trigger
The data acquisition boards offer a wide variety of trigger modes. Besides the standard signal checking for level and edge as known from oscilloscopes it's also possible to define a window trigger. All trigger modes could be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses.

External trigger I/O
All boards could be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulsewidth. An internally recognised trigger event could - activated by software - routed to the output connector to start external instruments.

Pulse width
Defines the minimum or maximum width that a trigger pulse could have to generate a trigger event. Could be combined with channel trigger, pattern trigger and external trigger.

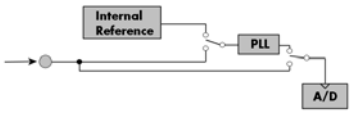
Multiple Recording


The Multiple Recording option allows the recording of several trigger events without restarting the hardware. With this option very fast repetition rates could be achieved. The on-board memory is divided in several segments of same size. Each of them is filled with data if a trigger event occurs.

Gated Sampling


The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level.

External clock I/O
Using an external connector a sampling clock could be fed in from an external system. It's also possible to put out the internally used sampling clock to synchronise external equipment to this clock.

Reference clock


The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Input impedance
All inputs could individually be switched by software between 50 Ohm and 1 MOhm input impedance. If using fast signals and high sampling rates or have 50 Ohm cable impedance the use of the 50 Ohm termination is recommended to minimise noise and signal reflections. If using weak signal sources or standard probes the use of the 1 MOhm termination is helpful.

Differential inputs
With a simple software command the inputs could individually be switched from single-ended (in relation to ground) to differential. When the inputs are used in differential mode the A/D converter measures the difference between two lines with no relation to system ground.

Technical Data

Resolution	16 bit	Dimension	160 mm x 100 mm (Standard 3U)
Differential linearity error	< 1 LSB (ADC)	Width (Standard board)	1 full size slot
Integral linearity error	< 2.5 LSB (ADC)		
Multi: Trigger to 1st sample delay	fixed	Connector	3 mm SMB male
Multi: Recovery time	< 20 samples	Inputs	Differential / Single Ended
ext. Trigger accuracy	1 Sample	Input impedance	50 Ohm / 1 MOhm || 25 pF
int. Trigger accuracy	1 Sample	Overvoltage protection	±40 V
input signal with 50 ohm termination	max 5 V rms	Warm up time	10 minutes
Trigger output delay	1 Sample	Operating temperature	0°C - 50°C
Offset error	< 1 LSB, adjustable by user	Storage temperature	-10°C - 70°C
Gain error	< 1%	Humidity	10% to 90%
Noise @ full speed, 50 ohm termination	< 2.5 LSB rms		
Crosstalk @ 20 kHz	< -95 dB	Power consumption -12 V	max. 50 mA (600 mWatt)
Ext. clock: delay to internal clock	42 ns ± 2 ns	Power consumption +12 V	max. 50 mA (600 mWatt)
		Power consumption 5 V @ full speed	max. 1.4 A (7.0 Watt)
Max common mode voltage	±8 V (differntial inputs)	Power consumption 5 V @ power down	max. 1.0 A (5.0 Watt)
Trigger input:Standard TTL level	Low: -0.5 > level < 0.8 V High: 2.0 V > level < 5.5 V Trigger pulse must be valid ≥ 2 clock periods.	Clock input: Standard TTL level	Low: -0.5 > level < 0.8 V High: 2.0 V > level < 5.5 V Rising edge is used. Required duty cycle: 50% ± 5%
Trigger output	Standard TTL, capable of driving 50 Ohm. Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -32 mA) One positive edge after the first internal trigger	Clock output	Standard TTL, capable of driving 50 Ohm Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -32 mA)

	MX.4520	MX.4530	MX.4540
Min internal clock	1 kS/s	1 kS/s	1 kS/s
Max internal clock	200 kS/s	500 kS/s	1 MS/s
Min external clock	DC	DC	1 kS/s
Max external clock	200 kS/s	500 kS/s	1 MS/s
-3 dB bandwidth	>100 kHz	>250 kHz	>500 kHz

Dynamic Parameters

	MX.4520	MX.4530	MX.4540
Test - Samplerate	200 kS/s	500 kS/s	1 MS/s
Testsignal frequency			
SNR (typ)			
THD (typ)			
SFDR (typ), incl harm.			
SINAD (typ)			
ENOB (based on SINAD)			

Dynamic parameters are measured at ± 1 V input range and 50 Ohm termination with the samplerate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

Order information

Order No	Description	Order No	Description
MX4520	MX.4520 with 8 MSample memory and drivers/SBench 5.x	MX4xxx-16M	Option: 16 MSample memory instead of 8 MSample standard mem
MX4530	MX.4530 with 8 MSample memory and drivers/SBench 5.x	MX4xxx-32M	Option: 32 MSample memory instead of 8 MSample standard mem
MX4540	MX.4540 with 8 MSample memory and drivers/SBench 5.x	MX4xxx-64M	Option: 64 MSample memory instead of 8 MSample standard mem
		MX4xxx-up	Additional handling costs for later memory upgrade
MX4xxx-mr	Option Multiple Recording: Memory segmentation		
MX4xxx-gs	Option Gated Sampling: Gate signal controls acquisition		
Cab-3f-9m-80	Adapter cable: SMB female to BNC male 80 cm	MX45xx-dl	DASYLab driver for MX.45xx series
Cab-3f-9m-200	Adapter cable: SMB female to BNC male 200 cm	MX45xx-hp	VEE driver for MX.45xx series
Cab-3f-9f-80	Adapter cable: SMB female to BNC female 80 cm	MX45xx-lv	LabVIEW driver for MX.45xx series
Cab-3f-9f-200	Adapter cable: SMB female to BNC female 200 cm	MATLAB	MATLAB driver for all MI.xxxx, MC.xxxx and MX.xxxx series.

technical changes and printing errors possible