



SPECTRUM

SYSTEMENTWICKLUNG MICROELECTRONIC GMBH

MC.72xx - 32 bit Digital Pattern Generator with programmable logic levels

- CompactPCI 6U format
- Programmable output levels from -2,0 V up to +10,0 V
- Levels individually programmable per 4 bit
- Up to 40 MS/s at 32 bit
- Possible use of memory saving 8 bit mode
- All Outputs can be separately disabled (Tristate)
- Hardware controlled differential output possible (8 bit and 16 bit)
- Up to 512 MByte on-board memory
- Output in FIFO mode
- Synchronization possible



Product range overview

Model	8 bit	16 bit	32 bit
MC.7210	10 MS/s	10 MS/s	
MC.7211	10 MS/s	10 MS/s	5 MS/s
MC.7220	40 MS/s	40 MS/s	
MC.7221	40 MS/s	40 MS/s	40 MS/s

Software/Drivers

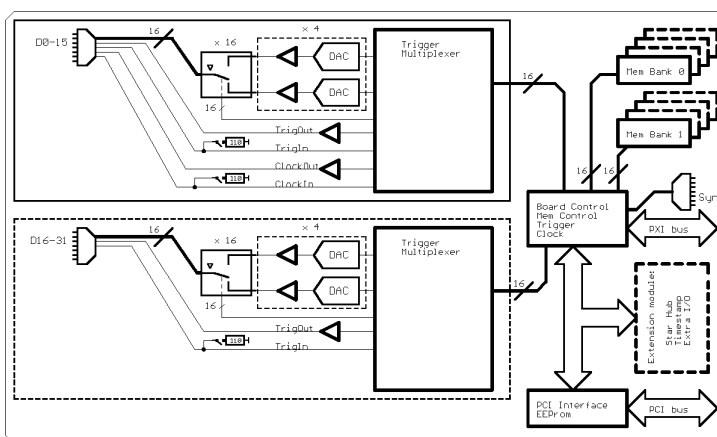
A large number of drivers and examples are delivered with the board or are available as an option:

- Windows 98/ME/NT/2000/XP - drivers
- Linux - drivers
- SBench 5.2
- Microsoft Visual C++ examples
- Borland Delphi examples
- Microsoft Visual Basic examples
- Microsoft Excel examples
- LabWindows/CVI examples
- FlexPro support with SBench
- LabVIEW - drivers (as option)
- DASyLab - drivers (as option)
- MATLAB - drivers (as option)
- Agilent VEE - drivers (as option)

General Information

The MC.72xx pattern generator series gives the user the possibility to generate digital data with a wide range of output levels. For every 4 bit the LOW and HIGH levels can be programmed from -2.0 V up to +10.0 V. Even at high speeds you are not limited concerning the maximum output swing. This enables the user to drive devices of nearly any logic family, like ECL, PECL, TTL, LVDS, LVTTTL, CMOS or LVCMOS. The potentially necessary differential signals are generated in hardware, so that only one data bit is used for each pair of differential signals. All outputs can be separately disabled allowing the easy connection with digital acquisition boards and the adaption to a wide range of test setups. The internal standard synchronization bus allows synchronisation of several MC.xxxx boards. Therefore the MC.72xx board could be used as an enlargement to any digital or analog board.

Hardware block diagram



Software programmable parameters

Samplerate	1 kS/s to max samplerate, external clock, ref clock
Output level	LOW/HIGH level p. nibble; -2,0 V up to +10,0 V in steps of 1mV
Clock mode	internal PLL, int.quartz, external, ext. divided, ext. reference clock
Clock impedance	110 Ohm / 50 kOhm
Trigger impedance	110 Ohm / 50 kOhm
Data Enable mask	programmable for every single bit
Trigger mode	External TTL, software
Memory depth	32 up to installed memory in steps of 32
Posttrigger	32 up to 256 M in steps of 32
Multiple Recording segmentsize	32 up to installed memory / 2 in steps of 32

Application examples

Semiconductor test	Production test	Burn-in test
Laboratory purposes	Pattern generator	Semiconductor development
Process control	ATE	

Possibilities and options

FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

External trigger I/O

All boards could be triggered using an external TTL signal. It's possible to use positive or negative edge. An internally recognised trigger event could - activated by software - routed to the output connector to start external instruments.

External clock I/O

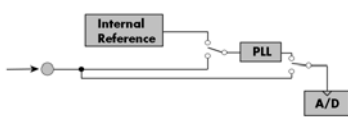
Using an external connector a sampling clock could be fed in from an external system. It's also possible to put out the internally used sampling clock to synchronise external equipment to this clock.

ECL Mode

When the ECL mode is activated, differential signals which are needed for e.g. ECL interfacing are generated in hardware on the odd data outputs. This results in the use of only one data bit for every pair of differential outputs and allows a very efficient use of memory.

Reference clock

The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock this way. The driver automatically generates the requested sampling clock from the fed in reference clock.



When the ECL mode is activated, differential signals which are needed for e.g. ECL interfacing are generated in hardware on the odd data

Cascading

The cascading option synchronises up to 4 Spectrum boards internally. It's the simplest way to build up a multi channel system. There is a phase delay between two boards of about 500 pico seconds when this synchronisation option is used.

Star hub

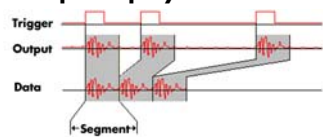
The star hub is an additional module allowing the phase stable synchronisation of up to 16 boards. Independent of the number of boards there is no phase delay between all channels. The star hub distributes trigger and clock information between all boards. As a result all connected boards are running with the same clock and the same trigger.

Extra I/O

The Extra I/O module adds 24 additional digital I/O lines and 4 analog outputs on an extra connector. These additional lines are independent from the standard function and could be controlled asynchronously. There is also an internal version available with 16 digital I/Os and 4 analog outputs that could be used directly at the rear board connector.

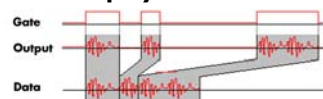
Multiple Replay

The Multiple Replay option allows the fast repetition output on several trigger events without restarting the hardware. With this option very fast repetition rates could be achieved. The on-board memory is divided in several segments of same size. Each of them is generated if a trigger event occurs.



Gated Replay

The Gated Sampling option allows data replay controlled by an external gate signal. Data is only replayed if the



gate signal has a programmed level.

Singleshot output

When singleshot output is activated the data of the on-board memory is replayed exactly one time. As trigger source one can use the external TTL trigger or the software trigger.

Continuous output

When continuous output is activated the data of the on-board memory is replayed continuously until a stop command is executed. As trigger source one can use the external TTL trigger or the software trigger.

Technical Data

Internal samplerate	1 kS/s up to maximum (depending on model)			Dimension	160 mm x 233 mm (Standard 6U)
External samplerate	DC up to maximum (depending on model)			Width (MC.721x)	1 slot
Clock input impedance	110 Ohm / 50 kOhm 15 pF			Width (MC.722x)	2 slots
Trigger input impedance	110 Ohm / 50 kOhm 15 pF			Output connector	40 pole half pitch (Hirose FX2 series)
Output impedance	approximately 80 Ohm			Power connector (MC.722x only)	soldered Y - cable with Molex 8981 (5,25" disc drive connector)
Data signal level	programmable from -2.0 V up to +10.0 V with an accuracy of ± 10 mV				
Output swing	0.1 ... 12.0 V				
	per pin	per nibble	per card	Operating temperature	0°C to 50°C
Maximum output current	100 mA	200 mA	0.5 A (MC.721x only)	Storage temperature	-10°C to 70°C
	1 MHz	40 MHz		Humidity	10% to 90%
Rise time ^a	2.00 ns	2.25 ns			
Fall time ^a	2.00 ns	2.25 ns			
Multi: Trigger to 1st sample delay	fixed				
Multi: Recovery time	< 20 samples (16 - 32 bit)				
	32 bit	16 bit	8 bit		
Trigger accuracy (samples)	1	1	2		

a. Tested with full output swing from -2.0 V to 10.0 V with no load

Trigger input: Standard TTL level	Low: -0.5 > level < 0.8 V High: 2.0 V > level < 5.5 V Trigger pulse must be valid ≥ 2 clock periods.	Clock input: Standard TTL level	Low: -0.5 > level < 0.8 V High: 2.0 V > level < 5.5 V Rising edge is used. Required duty cycle: 50% \pm 5%
Trigger output	Standard TTL, capable of driving 50 Ohm. Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -32 mA) One positive edge after the first internal trigger	Clock output	Standard TTL, capable of driving 50 Ohm Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -32 mA)

Power consumption (maximum value)	Full speed			Power down mode		
	+5 V (CPCI Bus)	+12 V (CPCI Bus)	+12 V (Connector)	+5 V (CPCI Bus)	+12 V (CPCI Bus)	+12 V (Connector)
MC.7210 (16 bit output @ 10 MS/s) ^a	1.5 A (7.5 W)	0.35 A (4.2 W)	-	1.3 A (6.5 W)	0,07 A (0.9 W)	-
MC.7211 (32 bit output @ 5 MS/s) ^a	1.8 A (9.0 W)	0.40 A (4.8 W)	-	1.5 A (7.5 W)	0.15 A (1.8 W)	-
MC.7220 (16 bit output @ 40 MS/s) ^b	1.8 A (7.5 W)	0 A	1.8 A (21.6 W)	1.6 A (8.0 W)	0 A	0.2 A (2.4 W)
MC.7221 (32 bit output @ 40 MS/s) ^b	2.5 A (12.5 W)	0 A	3.6 A (43.2 W)	2.2 A (11.0 W)	0 A	0.5 A (4.8 W)

a. Tested with full output swing from -2.0 to 10.0 V with no load

b. Tested with full output swing from -2.0 V to 10.0 V with 50 mA output current per pin

Order information

Order No	Description	Order No	Description
MC7210	MC.7210 with 16 MByte (128 MBit) memory, cables and drivers	MC7xxx-32M	Option: 32 MByte memory instead of 16 MByte standard mem
MC7211	MC.7211 with 16 MByte (128 MBit) memory, cables and drivers	MC7xxx-64M	Option: 64 MByte memory instead of 16 MByte standard mem
MC7220	MC.7220 with 16 MByte (128 MBit) memory, cables and drivers	MC7xxx-128M	Option: 128 MByte memory instead of 16 MByte standard mem
MC7221	MC.7221 with 16 MByte (128 MBit) memory, cables and drivers	MC7xxx-256M	Option: 256 MByte memory instead of 16 MByte standard mem
		MC7xxx-512M	Option: 512 MByte memory instead of 16 MByte standard mem
MC7xxx-smod	Star Hub: Synchronisation of 2 - 16 boards, one option per system	MC7xxx-up	Additional handling cost for later memory upgrade
MCxxxx-xmf	Extra I/O, external connector: 24 DI/O, 4 Analog out, incl. cable	MC7xxx-mr	Option Multiple Replay: Memory segmentation
		MC7xxx-gs	Option Gated Replay: Gate signal controls replay
MC72xx-dl	DASYLab driver for MC.72xx series	MC7xxx-cs	Synchronisation of 2 - 4 boards, one option per system
MC72xx-hp	VEE driver for MC.72xx series		
MC72xx-lv	LabVIEW driver for MC.72xx series	MCxxxx-dcab	Additional 40 pole flat ribbon cable with IDC socket connector, ca. 1 m
MATLAB	MATLAB driver for all MI.xxxx, MC.xxxx and MX.xxxx series.	MCxxxx-dcab2	Additional 40 pole flat ribbon cable with Fx2 connector, ca. 1 m

technical changes and printing errors possible