



SPECTRUM

SYSTEMENTWICKLUNG MICROELECTRONIC GMBH

MC.30xx - 12 bit transient recorder up to 200 MS/s

- CompactPCI / PXI 6U format
- Fastest 12 bit A/D converter board
- Up to 200 MS/s on 1 channel
- Up to 100 MS/s on 2 channels
- Up to 60 MS/s on four channels
- Simultaneously sampling on all channels
- 6 input ranges: ± 200 mV up to ± 10 V
- Up to 256 MSample memory
- FIFO mode for slower samplerates
- Window and pulsewidth trigger
- Input offset up to $\pm 100\%$
- Synchronization possible

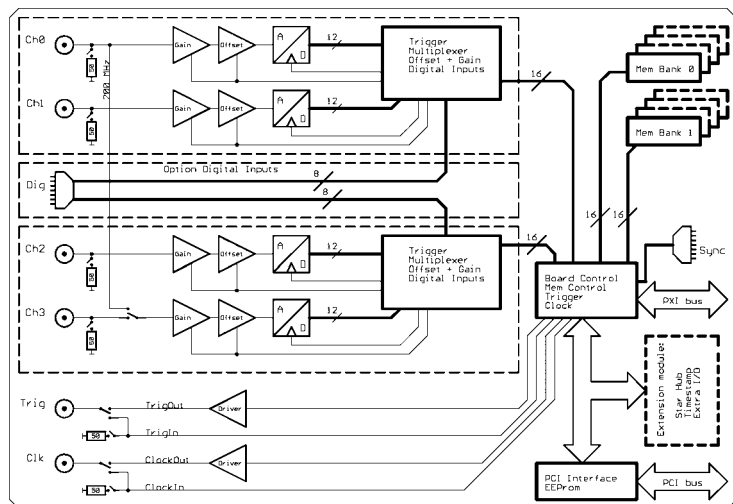


Product range overview

All 16 boards of the MC.30xx series may use the on-board memory completely for the currently active number of channels.

Model	1 channel	2 channels	4 channels
MC.3010	80 MS/s		
MC.3011	40 MS/s	40 MS/s	
MC.3012	80 MS/s	40 MS/s	
MC.3013	40 MS/s	40 MS/s	40 MS/s
MC.3014	80 MS/s	80 MS/s	40 MS/s
MC.3015	160 MS/s	80 MS/s	
MC.3016	160 MS/s	80 MS/s	40 MS/s
MC.3020	100 MS/s		
MC.3021	50 MS/s	50 MS/s	
MC.3022	100 MS/s	50 MS/s	
MC.3023	50 MS/s	50 MS/s	50 MS/s
MC.3024	100 MS/s	100 MS/s	50 MS/s
MC.3025	200 MS/s	100 MS/s	
MC.3026	200 MS/s	100 MS/s	50 MS/s
MC.3027	100 MS/s	100 MS/s	
MC.3031	60 MS/s	60 MS/s	
MC.3033	60 MS/s	60 MS/s	60 MS/s

Hardware block diagram



Software/Drivers

A large number of drivers and examples are delivered with the board or are available as an option:

- Windows 98/ME/NT/2000/XP - drivers
- Linux - drivers
- SBench 5.2
- Streaming Software SPviewIT 6.2(as option)
- Microsoft Visual C++ examples
- Borland Delphi examples
- Microsoft Visual Basic examples
- Microsoft Excel examples
- LabWindows/CVI examples
- FlexPro support with SBench
- LabVIEW - drivers (as option)
- DASYLab - drivers (as option)
- MATLAB - drivers (as option)
- Agilent VEE - drivers (as option)

Software programmable parameters

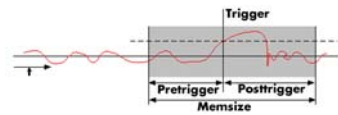
Samplerate	1 kS/s to max samplerate, external clock, ref clock
Input Range	± 200 mV, ± 500 mV, ± 1 V, ± 2 V, ± 5 V, ± 10 V
Input impedance	50 Ohm / 1 MOhm
Input Offset	$\pm 100\%$ in steps of 1%
Clock mode	internal PLL, int.quartz, external, ext. divided, ext. reference clock
Clock impedance	50 Ohm / 1 MOhm
Trigger impedance	50 Ohm / 1 MOhm
Trigger mode	Channel, External, Software, Auto, Windows, Pulse
Trigger level	1/256 to 255/256 of input range
Trigger edge	rising edge, falling edge or both edges
Trigger pulsewidth	1 to 255 samples in steps of 1 sample
Memory depth	32 up to installed memory in steps of 32
Posttrigger	32 up to 128 M in steps of 32
Multiple Recording segmentsize	32 up to installed memory / 2 in steps of 32

Application examples

LDA/PDA	Production test	Laboratory equipment
Radar	Spectroscopie	Test of mobile communication
Ultrasound	Medical equipment	

Possibilities and options

Ring buffer mode



The ring buffer mode is the standard mode of all oscilloscope boards. Data is written in a ring memory of the board until a trigger event is

detected. After the event the posttrigger values are recorded. Because of this continuously recording in a ring buffer there are also samples prior to the trigger event visible: Pretrigger = Memsiz - Posttrigger.

FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

Channel trigger

The data acquisition boards offer a wide variety of trigger modes. Besides the standard signal checking for level and edge as known from oscilloscopes it's also possible to define a window trigger. All trigger modes could be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses.

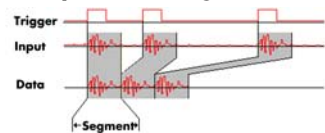
External trigger I/O

All boards could be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulsewidth. An internally recognised trigger event could - activated by software - routed to the output connector to start external instruments.

Pulse width

Defines the minimum or maximum width that a trigger pulse could have to generate a trigger event. Could be combined with channel trigger, pattern trigger and external trigger.

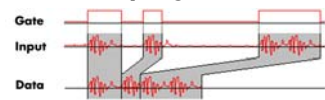
Multiple Recording



The Multiple Recording option allows the recording of several trigger events without restarting the hardware. With this option very fast repetition rates could be achieved. The

on-board memory is divided in several segments of same size. Each of them is filled with data if a trigger event occurs.

Gated Sampling



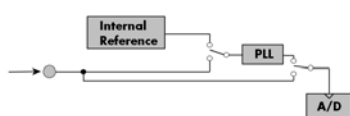
The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a pro-

grammed level.

External clock I/O

Using an external connector a sampling clock could be fed in from an external system. It's also possible to put out the internally used sampling clock to synchronise external equipment to this clock.

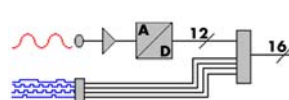
Reference clock



The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality mea-

surements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Digital inputs



This option acquires additional synchronous digital channels phase-stable with the analog data. When the option is installed there are 4 additional digital inputs for every analog A/D channel.

Cascading

The cascading option synchronises up to 4 Spectrum boards internally. It's the simplest way to build up a multi channel system. There is a phase delay between two boards of about 500 pico seconds when this synchronisation option is used.

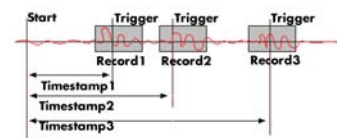
Star hub

The star hub is an additional module allowing the phase stable synchronisation of up to 16 boards. Independent of the number of boards there is no phase delay between all channels. The star hub distributes trigger and clock information between all boards. As a result all connected boards are running with the same clock and the same trigger.

Extra I/O

The Extra I/O module adds 24 additional digital I/O lines and 4 analog outputs on an extra connector. These additional lines are independent of the standard function and could be controlled asynchronously. There is also an internal version available with 16 digital I/Os and 4 analog outputs that could be used directly at the rear board connector.

Timestamp



The timestamp option writes the time positions of the trigger events in an extra memory. The timestamps are relatively to the start of recording, to a defined zero time

or externally synchronised to a radio clock or a GPS receiver. With this option acquisitions of systems on different locations could be set in a precise time relation.

Technical Data

Resolution	12 bit	Input signal with 50 Ohm termination	max 5 V rms
Differential linearity error	≤ 1 LSB (ADC)	Input impedance	50 Ohm / 1 MOhm 25 pF
Integral linearity error	≤ 1 LSB (ADC)	Overvoltage protection (range ≤ ±1 V)	±5 V
Offset error	adjustable by user	Overvoltage protection (range > ±1 V)	±50 V
Gain error	< 1%	Digital Inputs input impedance	110 Ohm @ 2.5 V
Crosstalk 1 MHz signal, 50 Ohm term	< -70 dB	Digital Inputs delay to analog sample	-12 samples
Multi: Trigger to 1st sample delay	-10 to +20 samples (fix)	Dimension	160 mm x 233 mm (6U standard)
Multi: Recovery time	< 20 samples	Width (Standard)	1 slot
ext. Trigger accuracy (<125 MS/s)	1 Samples	Width (with digital inputs or star hub)	2 slots
ext. Trigger accuracy (>160 MS/s)	2 Samples	Connector	3 mm SMB male
int. Trigger accuracy	1 Sample	Warm up time	10 minutes
Trigger output delay		Operating temperature	0°C - 50°C
Ext. clock: delay to internal clock	42 ns ± 2 ns	Storage temperature	-10°C - 70°C
Min internal clock	1 kS/s	Humidity	10% to 90%
Min external clock	1 MS/s	Power consumption 5 V @ full speed	max 3.4 A (17.0 Watt)
		Power consumption 5 V @ power down	max. 2.3 A (11.5 Watt)

Trigger input: Standard TTL level	Low: -0.5 > level < 0.8 V High: 2.0 V > level < 5.5 V Trigger pulse must be valid ≥ 2 clock periods.	Clock input: Standard TTL level	Low: -0.5 V > level < 0.8 V High: 2.0 V > level < 5.5 V Rising edge. Duty cycle: 50% ± 5%
Trigger output	Standard TTL, capable of driving 50 Ohm. Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -32 mA) One positive edge after the first internal trigger	Clock output	Standard TTL, capable of driving 50 Ohm Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -32 mA)

	MC.3011 MC.3013	MC.3021 MC.3023	MC.3031 MC.3033	MC.3010 MC.3012 MC.3014	MC.3020 MC.3022 MC.3024 MC.3027	MC.3015 MC.3016	MC.3025 MC.3026
max internal clock	40 MS/s	50 MS/s	62.5 MS/s	80 MS/s	100 MS/s	160 MS/s	200 MS/s
max external clock	40 MS/s	50 MS/s	62.5 MS/s	80 MS/s	100 MS/s	80 MS/s	100 MS/s
-3 dB bandwidth	> 20 MHz	> 25 MHz	> 30 MHz	> 40 MHz	> 40 MHz	> 40 MHz	> 40 MHz
Zero noise level (< 125 MS/s)	< 1.5 LSB rms	< 1.5 LSB rms	< 1.75 LSB rms	< 2.0 LSB rms	< 2.0 LSB rms	< 2.0 LSB rms	< 2.0 LSB rms
Zero noise level (> 125 MS/s)	n.a.	n.a.	n.a.	n.a.	n.a.	< 3.0 LSB rms	< 3.0 LSB rms

Dynamic Parameters

	MC.3011 MC.3013	MC.3021 MC.3023	MC.3031 MC.3033	MC.3010 MC.3012 MC.3014	MC.3020 MC.3022 MC.3024 MC.3027	MC.3015 MC.3016	MC.3025 MC.3026
Test - Samplerate	40 MS/s	50 MS/s	60 MS/s	80 MS/s	100 MS/s	80 MS/s	100 MS/s
Testsignal frequency	1 MHz	1 MHz	1 MHz	1 MHz	1 MHz	1 MHz	1 MHz
SNR (typ)	> 64.8 dB	> 64.8 dB	> 63.3 dB	> 64.8 dB	> 64.7 dB	> 64.8 dB	> 63.9 dB
THD (typ)	< -73.8 dB	< -73.8 dB	< -73.2 dB	< -73.8 dB	< -73.8 dB	< -73.9 dB	< -73.5 dB
SFDR (typ), excl harm.	> 77.5 dB	> 77.5 dB	> 74.3 dB	> 77.1 dB	> 76.8 dB	> 77.0 dB	> 74.3 dB
SINAD (typ)	> 64.3 dB	> 64.3 dB	> 62.9 dB	> 64.3 dB	> 64.2 dB	> 64.3 dB	> 63.4 dB
ENOB (based on SINAD)	> 10.4 LSB	> 10.4 LSB	> 10.2 LSB	> 10.4 LSB	> 10.4 LSB	> 10.4 LSB	> 10.2 LSB

Dynamic parameters are measured at ± 1 V input range (if no other range is stated) and 50 Ohm termination with the samplerate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

Order information

Order No	Description	Order No	Description
MC3010	MC.3010 with 8 MSample memory and drivers/SBench 5.x	MC3xxx-16M	Option: 16 MSample memory instead of 8 MSample standard mem
MC3011	MC.3011 with 8 MSample memory and drivers/SBench 5.x	MC3xxx-32M	Option: 32 MSample memory instead of 8 MSample standard mem
MC3012	MC.3012 with 8 MSample memory and drivers/SBench 5.x	MC3xxx-64M	Option: 64 MSample memory instead of 8 MSample standard mem
MC3013	MC.3013 with 8 MSample memory and drivers/SBench 5.x	MC3xxx-128M	Option: 128 MSample memory instead of 8 MSample standard mem
MC3014	MC.3014 with 8 MSample memory and drivers/SBench 5.x	MC3xxx-256M	Option: 256 MSample memory instead of 8 MSample standard mem
MC3015	MC.3015 with 8 MSample memory and drivers/SBench 5.x	MC3xxx-up	Additional handling costs for later memory upgrade
MC3016	MC.3016 with 8 MSample memory and drivers/SBench 5.x		
MC3020	MC.3020 with 8 MSample memory and drivers/SBench 5.x	MC3xxx-mr	Option Multiple Recording: Memory segmentation
MC3021	MC.3021 with 8 MSample memory and drivers/SBench 5.x	MC3xxx-gs	Option Gated Sampling: Gate signal controls acquisition
MC3022	MC.3022 with 8 MSample memory and drivers/SBench 5.x	MC3xxx-dig	Additional 4 synchronous digital inputs per channel, incl. cable
MC3023	MC.3023 with 8 MSample memory and drivers/SBench 5.x	MC3xxx-cs	Synchronisation of 2 - 4 boards, one option per system
MC3024	MC.3024 with 8 MSample memory and drivers/SBench 5.x	MC.30xx-hbw	100 MHz bandwidth for MC.3025/26 at fixed ±500 mV input
MC3025	MC.3025 with 8 MSample memory and drivers/SBench 5.x	MC30xx-dl	DASYLab driver for MC.30xx series
MC3026	MC.3026 with 8 MSample memory and drivers/SBench 5.x	MC30xx-hp	VEE driver for MC.30xx series
MC3027	MC.3027 with 8 MSample memory and drivers/SBench 5.x	MC30xx-lv	LabVIEW driver for MC.30xx series
MC3031	MC.3031 with 8 MSample memory and drivers/SBench 5.x	MATLAB	MATLAB driver for all MI.xxxx, MC.xxxx and MX.xxxx series.
MC3033	MC.3033 with 8 MSample memory and drivers/SBench 5.x	MC3xxx-time	Timestamp option: Extra memory for trigger time
MC3xxx-smod	Star Hub: Synchronisation of 2 - 16 boards, one option per system	Cab-3f9m-200	Adapter cable: SMB female to BNC male 200 cm
MCxxxx-xmf	Extra I/O, external connector: 24 DI/O, 4 Analog out, incl. cable	Cab-3f9f-80	Adapter cable: SMB female to BNC female 80 cm
Cab-3f9m-80	Adapter cable: SMB female to BNC male 80 cm	Cab-3f9f-200	Adapter cable: SMB female to BNC female 200 cm

technical changes and printing errors possible